REMARKS/ARGUMENTS

Claims 1-13 are pending in this application, new claims 11-13 having been added.

In the final office action, all the claims are rejected on the basis of Messerly either alone or in combination with other references.

The office action acknowledged that Messerly is directed to an interface device between a UART and a host DSP, rather than a UART according to the present invention. However, the Examiner stated that the structural elements and functions claimed in claim 1 were the same as in Messerly. The independent claims have now been amended to specifically set forth the different structural elements corresponding to the different functions of Messerly and the present invention.

The present invention.

The present invention is directed to a UART which transmits serial data over a transmission line. A FIFO buffer stores the data, and when it is empty, the UART sends a control signal relating to the availability of a serial transmission line. The embodiment in the application describes an RTS (Request to Send) signal to indicate the UART is through sending this data and is ready to receive data from the remote device. Users of UARTs usually program in the delay time to account for the quality and length of the transmission line, as well as variations in the length of the last word sent. The present invention addresses this by triggering a delay circuit from both a programmable register programmed by the customer, and a detection of the transmission of the last word. In the preferred embodiment, the stop bit of the last word is detected, rather than the start bit as in the prior art. This thus accounts of for variations in word length.

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Messerly describes an interface between a UART and a DSP. In particular, Messerly interfaces between a UART in a CPU and a DSP in a modem which is connected to phone line. The purpose of Messerly is to buffer the data to account for variations in speed between a CPU and DSP. In addition, Messerly, through this buffering system, reduces the

number of interrupts to allow the CPU and DSP to perform other functions without constantly attending to the handling of this transmission of data. As can be seen from Figure 1, the Messerly interface device (UDIF) 110 is connected by parallel ports to both the UART and to the DSP. The references to serial transmission in the patent refer to the emulation of a serial transmission by controlling the speed of transmission to correspond to that a serial link.

Distinctions in amended claims.

Claim 1 has been added to clarify that the invention is directed to a serial transmission. In particular, claim 1 now specifically sets forth the shift register which is connected to the FIFO buffer (this is shown as shift register 40 in Figure 2). Claim 1 also specifically claims the serial transmission line which is coupled to the shift register (42 in Figure 2). As noted above, Messerly uses a parallel interface, and does not use a serial interface. The references to emulating a serial interface in Messerly are references to controlling the speed so it corresponds to the speed of serialized data (see, e.g., col. 3, ll. 49-52, col. 5 ll. 17-23, col. 8, ll. 57-61, and col. 13, ll. 44-56). They are not references to using a serial transmission line.

Claim 1 has also been amended to clarify that the "transmitter empty" signal is the control signal relating to the availability of a serial transmission line. This does not add new matter since one such signal is the RTS signal shown on pin 54 of Figure 2. As described above, this signal indicates to a remote device that the UART is finished transmitting since the last word in the FIFO has been detected. This indicates that the remote device can now transmit. The use of the programmable register and the detection of the last word allow optimization to minimize the delay between a transmission in one direction and a reception of data from a transmission by the remote device.

Messerly, on the other hand, does not discuss controlling a delay in connection with a control signal such as an RTS signal. The only place in Messerly where the RTS signal is mentioned is in col. 7, line 16, referring to different status signals from the UART. The delay discussed in Messerly is the delay required to control the transmission time of the data for purposes such as emulating a serial connection by slowing down the data appropriately. In addition, the determination of this delay timing is not done by the interface device of Messerly,

but rather is done by the DSP which reads a register in the interface device, performs a calculation, and determines the appropriate timing. This is what is discussed in col. 12, ll. 50-67 and col. 13, ll. 1-21. In particular, in col. 12, ll. 53-56 it is stated that, "In Fig. 1, the DSP 112 determines the character time for the UART 108 by reading the DIVL and performing the appropriate calculations." As explained in that same paragraph, this is used to determine the character time, which is the amount of time needed to transmit one character at the baud rate specified by the host computer through the divisor latch (DIVL).

Thus, Messerly is directed to something completely different from the present invention, the idea of pacing the character time so that it emulates the pacing of a serial transmission. Not only is this aspect different, but the calculation is actually done by the DSP, which is external to the interface device of Messerly, and is accessed over a parallel bus.

Accordingly, Messerly does not show the delaying of a control (e.g., RTS) signal, and the delay that it does show is performed externally to the device for an entirely different purpose, that of pacing the data, not for the purpose of determining when the transmission in the first direction will be completed and a transmission back in the other direction can be started. Such transmission line delays are not even an issue in Messerly, because the UART and the interface are local to the DSP and thus there is no transmission line or transmission line delay to be dealt with. The transmission line in Messerly is the phone line connected to the modem, which is on the other side of the interface device and the UART.

This further distinction is also reflected in the amendment to the claims, which set forth that the serial transmission line is connected to a remote processor. Again, no new matter is added since this is discussed, for example, in the first four paragraphs in the Background of the application.

Thus Messerly does not show, as now set forth in claim 1, that a last word transmitted is detected, that the detected last word is sent over a serial transmission line, that the detected last word is detected as it is being transmitted to a remote device, and that the detected last word is used to trigger the control signal. Claim 1 is thus believed allowable over Messerly.

Claim 2.

Claim 2 specifies detection of the stop bit of the last word transmitted from the FIFO buffer, and has been amended to clarify that the transmitter empty signal is in fact the control signal. The office action acknowledged that Messerly does not show generating a signal from the stop bit of a last word, but suggested it would be obvious to do so. However, since Messerly is directed to a different issue as discussed above, it is submitted that it would not be obvious to modify Messerly to trigger its timing signal from the stop bit since Messerly is directed to the correct pacing of the data, not to when the end of a last data word is transmitted, as in the present invention. In addition, as noted above, Messerly does not teach triggering a delay from the control (e.g., RTS) signal. Accordingly, for these reasons, in addition to the reasons set forth above, claim 2 is believed to be allowable over the cited art.

Claim 11.

New claim 11 is dependent upon claim 2, and further sets forth that the stop bit is detected in the shift register, not in the FIFO buffer. This can be seen in one embodiment from the drawing of Figure 2, which shows the stop bit detect circuit 46 connected to shift register 40. As noted above, the circuitry of Messerly uses a parallel interface, and thus does not have a shift register at all to trigger generating any delay signal. In addition, there is no circuitry shown or suggested in Messerly to connect to a shift register, or the FIFO for that matter, to detect a stop bit of the last word. Accordingly, for these reasons and the reasons set forth above, claim 11 is believed to be allowable over the cited art.

Claim 12.

New claim 12 specifies that the control signal of claim 1 is the RTS signal. As discussed above, this is not show or suggested by Messerly, which only mentions the RTS signal once, and not in connection with any delay.

Claim 13.

Claim 13 is a new independent claim similar to claim 1, but further setting forth that the last word transmitted from the shift register is detected, as opposed to claim 1, which

claims detecting the last word transmitted from the FIFO, whether it subsequently goes through a shift register or not. Messerly does not show or suggest detecting the last word transmitted from a shift register.

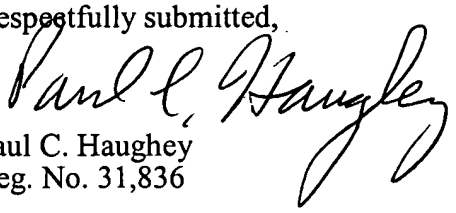
The remaining claims are believed allowable for the same reasons, and for showing additional combinations not shown or suggested by Messerly or the other cited art.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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